The Transport and Isolation Properties of Polycrystalline GaAs Selectively Grown by Molecular Beam Epitaxy

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Abstract—**Selective-area polycrystalline GaAs using SiO_2 masking is planarly grown by molecular beam epitaxy (MBE). The electric properties of the polycrystalline GaAs are investigated because this technology is very promising for device isolation in GaAs integrated circuit and electro-optic integration. Compared with the isolation characteristics of semi-insulating GaAs, polycrystalline GaAs has similar low-field resistivity, higher high-field leakage current, and no well-defined trap-fill-limited voltage. The grain boundary (GB) states of polycrystalline GaAs trap negative charge that builds up a potential barrier to hinder electron current. The GB density of states profile estimated from the *I-V* characteristics shows a peak value 5×10^{12} cm$^{-2}\cdot$eV^{-1} and a wide energy distribution, 0.33 eV above the equilibrium Fermi energy.**

SELECTIVE epitaxial growth of GaAs has long been investigated for its potential application in integrated circuits by different epitaxial growth techniques such as LPE, VPE, and MBE. Among them, SiO_2 masked molecular beam epitaxy (MBE) growth has demonstrated its unique advantage over VPE and LPE by its precise film thickness control and excellent lateral uniformity [1].

Even though polycrystalline GaAs grown on SiO_2 has high low-field resistivity, we require low leakage current in the polycrystalline under high-field or high-bias condition when used in integrated circuits for isolation purposes. Since the voltage drop in polycrystalline GaAs is principally at the grain boundaries, carrier transport across grain boundaries determines the current flow in GaAs polycrystals. In this paper, we will investigate the property of the grain boundary first, and then study the physics of grain boundaries as regards the transport properties of polycrystalline GaAs. Finally, we will compare polycrystalline GaAs with semi-insulating GaAs based on the fundamental device physics.

In our experiment, 2000-Å thick SiO_2 is selectively deposited on an undoped LEC (100) GaAs wafer by PECVD. After normal pre-MBE wafer cleaning steps, a 1.7-μm selective single/poly crystalline GaAs is grown. The detailed growth conditions and TEM pictures of the grain microstructures are published elsewhere [2]. The SiO_2 region is single crystal with donor doping concentration 4×10^{17} cm^{-3} and low-field mobility 3500 cm^2/s$\cdot$V. The low-field resistivity of polycrystalline GaAs is 4×10^6 $\Omega\cdot$cm, which is about the same order as that of semi-insulating GaAs.

While the bias voltage across polycrystalline GaAs is increased, the current shows very nonlinear varistor characteristics. A parameter α defined as $\alpha = d(\ln I)/d(\ln V)$ is generally used to measure the degree of nonlinearity of a varistor. As shown in Fig. 1, the varistor parameter steeply increases to a very high peak value (>15), which implies that some breakdown takes place around that bias. As proposed by other researchers [3], the grain-boundary (GB) density of states profile can be estimated from the $I-V$ characteristics and the varistor parameter as follows if barrier lowering is responsible for the high current injection, and if only majority carriers are important:

$$n_s(qV_1+E_{f0}) = \sqrt{\frac{\epsilon N_D}{2q}} \cdot \left[\left(\frac{V}{\alpha V_t}-1\right)\frac{1}{\sqrt{V+V_{bi}-V_1}} - \frac{1}{\sqrt{V_{bi}-V_1}}\right] \quad (1a)$$

$$I = G_0 V_t e^{V_1/V_t}, \qquad V \gg V_t \quad (1b)$$

where n_s is the density of the GB states (cm$^{-2}\cdot$eV^{-1}), V_{bi} is the equilibrium built-in potential, V_1 is the change in the forward-bias barrier height from the equilibrium value, V is the applied bias on a single grain boundary, E_{f0} is the equilibrium Fermi energy (eV), $V_t = kT/q$, and G_0 is the measured low-field conductance.

The V_{bi} in (1a), measured by the varying temperature method [4], is 0.35 V. The GB density of states profile above E_{f0}, as determined from (1), is plotted in Fig. 2. Although it is not possible to obtain from (1) the information about GB density of states profile below E_{f0}, we can calculate the total amount of the occupied states at zero bias from the charge neutrality condition. Defining N_s and N_0 as the states above and below the zero-biased Fermi energy, we find $N_s = 1.05 \times 10^{12}$ cm^{-2} and $N_0 \approx 2.77 \times 10^{12}$ cm^{-2}. That means 70 percent of the GB states are occupied at zero bias to form the potential barrier that produces very high low-field resistance

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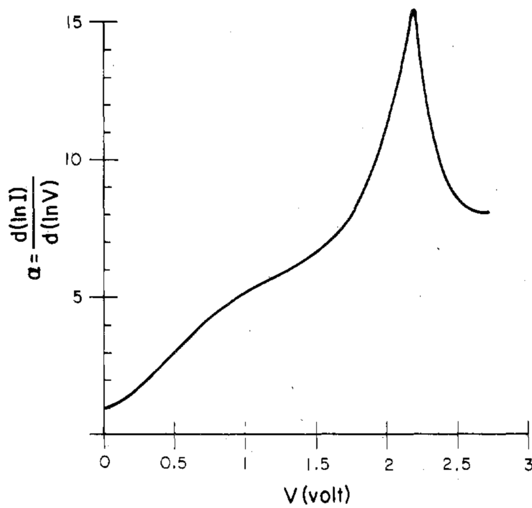

Fig. 1. Varistor parameter versus the applied voltage on a single grain boundary. The steep rise of α to the maximum implies the occurrence of GB-states full occupation, and the subsequent drop of α is mainly due to the series resistance. The voltage shown here is the average voltage drop on a single grain boundary.

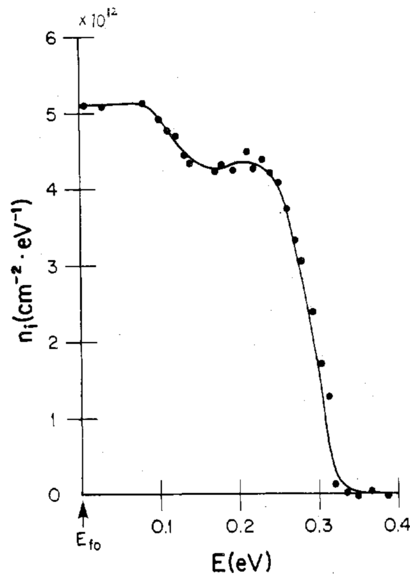

Fig. 2. GB density of states profile. The origin is assumed at the equilibrium Fermi energy. The profile smoothly changes until 0.26 eV from the origin and then sharply decreases to zero around 0.33 eV.

even though the doping concentration is quite high. As the bias is increased, more and more GB states are occupied and the barrier height of the forward-bias side is reduced. When the states in the grain boundary are rapidly filled, the current rises abruptly. The calculated GB-states-filled voltage for a single-grain boundary is 2.6 V, which is quite close to the value of 2.2 V from Fig. 1, where the varistor parameter α is highest. The deviation is principally caused by the tunneling current that has been neglected in our calculation.

Another possible breakdown mechanism of a grain boundary could be the impact ionization which can be physically modeled as the breakdown voltage of a very thin base bipolar transistor if we treat the narrow grain boundary as the base of a bipolar transistor. Because the carrier recombination velocity at the grain boundary, $\approx 10^4$ to 10^6 cm/s, is usually much smaller than the electron injection velocity, $\approx 10^7$ cm/s, the breakdown voltage is lower than the value of a one-sided junction by a factor $(\sigma N)^{1/n}$, where σ is the capture cross section of the recombination center, N is the total number of recombination centers in the grain boundary, and n is an empirical value between 4 and 6. The ratio of the GB-states-filled voltage and avalanche breakdown voltage of a grain boundary is formulated by (2) [5]

$$\frac{V_B}{V_P} = K \cdot \left[\frac{(\sigma N)^{1/n}}{N^2} \right] \tag{2}$$

where $\sigma \approx 10^{-14}$ cm^2, $N = N_s + N_0$ is the total GB states in a single grain boundary, and K, a constant almost independent of the doping concentration, is 3.4×10^{25} cm^{-4} for GaAs. From (2), GB-states full occupation is responsible for the abrupt current rise in the small and medium angle boundaries ($N = 10^{10} \rightarrow 10^{13}$ cm^{-2}), but avalanche breakdown becomes dominant in large-angle grain boundaries ($N > 10^{13}$ cm^{-2}).

In comparison of polycrystalline GaAs with semi-insulating GaAs, two drastic differences exist even though both polycrystalline GaAs and semi-insulating GaAs contain a number of deep levels that principally cause high resistivity. First, the deep levels in semi-insulating GaAs are uniformly distributed. On the contrary, the deep levels in polycrystalline GaAs are clustered at the grain boundary (that occupies only a few thousandths of the physical dimension). Secondly, the deep levels (EL_2) in semi-insulating GaAs have a fixed energy in the forbidden band [6], but as shown in Fig. 2 the deep levels at the grain boundary cover a much wider energy range. The fixed energy trap infers a well-defined trap-fill-limited voltage already clearly observed in semi-insulating GaAs in Fig. 3 [6]. The wide energy bandwidth of GB states in polycrystalline GaAs smears out the abrupt current change and as a result blurs the definition of trap-fill-limited voltage. The density of EL_2 level in semi-insulating GaAs can be determined by (3) [6], [7]

$$V_{TF} = \frac{qd}{2\epsilon} \cdot N_t. \tag{3}$$

It is found from (3) that $N_t = 9 \times 10^{10}$ cm^{-2}, corresponding to a volume concentration $n_t = 9 \times 10^{13}$ cm^{-3}, which is very low compared with the EL_2 concentration of undoped semi-insulating LEC wafers in which n_t varies from 5×10^{15} to 2×10^{16} cm^{-3} [8]. This is attributed to the depletion of EL_2 level near the substrate surface after thermal annealing [9]. On the other hand, (3) cannot be directly applied to polycrystalline GaAs since it will overestimate the V_{TF} to 1700 V! It is the very nonuniform spacial distribution of deep levels in polycrystalline GaAs that modifies (3). Since the deep levels are clustered around the grain boundaries, only the grain boundary contributes to isolation so that the physical dimension d in (3) should be replaced by the depletion width of a single grain boundary. Finally, the current level of polycrystalline GaAs in this region $V > V_{TF}$ is more than 1000 times higher than that of semi-insulating GaAs even though their low field resistivities are of the same order. After the bias is raised above its

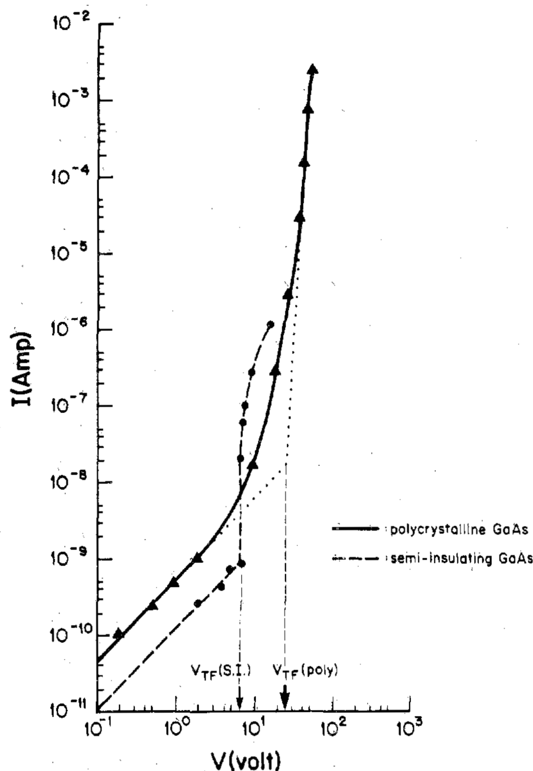

Fig. 3. I–V characteristics of GaAs polycrystal and semi-insulator. The physical lengths for both materials are 10 μm. The average grain size of the polycrystalline GaAs is 5000 Å. The former has much higher high-field leakage current but no well-defined trap-fill-limited voltage.

trap-fill-limited voltage, the semi-insulating GaAs is still resistive in space-charge region; on the contrary, n-type polycrystalline GaAs becomes very conductive once the GB states are fully occupied.

In summary, the GB density of states in polycrystalline GaAs is found to have a 0.33-eV bandwidth above the equilibrium Fermi energy and has a peak value 5×10^{12} $cm^{-2} \cdot eV^{-1}$ for a single grain boundary. This rather high total GB states, 3.8×10^{12} cm^{-2}, explains its semi-insulating property even at high doping levels. The isolation properties of GaAs polycrystal such as low-field resistivity, high-field leakage current, and trap-fill-limited voltage are compared with the GaAs semi-insulator. The comparable low-field resistivity ($10^6 \rightarrow 10^7$ Ω·cm), a much higher high-field current (>1000 times), and a less sharply defined trap-fill-limited voltage are obtained in polycrystalline GaAs. All these factors should be considered in the design of the GaAs integrated circuit by MBE selective growth.

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